8150dn manual

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Book Descriptions:

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Marvell PXA166 or PXA168 This board provides a second ethernet using the port provided by the macrocontrollers ethernet switch.For users in Windows or OSX we recommend virtualizing a Linux PC. Most of our platforms run Debian and if there is no personal distribution preference this is what we recommend for ease of use.Development will include accessing drives formatted for Linux and often Linux based tools.Disconnect the power source before moving, cabling, or performing any set up procedures. Inappropriate handling may cause damage to the board.Every DIO pin can source up to 12mA from the FPGA.Creating this connection is described more in the next chapter, but the first output is from the bootromThe first dot means the MBR was copied into memory and executed. The next two dots indicate that the MBR executed and the kernel and initrd were found and copied to memory.The first interface eth0 is configured to use IPv4LL, and eth00 is configured to use DHCP.In this case you can connect to either ts47104f47a5 or ts47104f47a5.OSX also comes preinstalled with the same command. Once this is installed you can runIn this case you can connect to either ts47104f47a5.local or ts47104f47a5.local.You will need a NULL MODEM cable.Be sure to replace the serial device string with that of the device on your workstation.Open up Device Manager to determine your console port. See the putty configuration image for more details.Booted in 0.90s. Initramfs Web Interface The initramfs is built into the kernel image so it cannot be modified without rebuilding the kernel, but it does read several bits from nonvolatile memory for common configuration options we call soft jumpers. Note Soft jumper settings are not stored on the SD media, so reflashing your SD card will not reset the soft jumpers. This action can only be taken from within the OS.Ensure that alternate access methods telnet, SSH, etc.http://www.aynispirit.nl/userfiles/caldina-st215-owners-manual.xml

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are set up and working in Debian if the serial port is not a viable access method before this jumper is set.You can also use tshwctlIf you do not have a serial console, make sure you first configure Debians network settings first before booting directly to Debian.The initramfs itself cannot be easily modified, and it is not recommended to do so. The initramfs however has several hooks for applications to manipulate its behavior. The init file does not exist by default and must be created.The xinit file is used to start up a window manager and any applications. The default initramfsxinit starts a webbrowser viewing localhostIf the xinit script ever closes, x11 will close. This is why the last This setting prevents. By default it is configured to. You can reduce this by specifying a polling rate. You can restrict this to. This is intended for production or updates. Most flash media based drives can be detected Debian provides many more packages and a much more familiar environment for users already versed in Debian. Through Debian it is possible to configure the network, use the aptget suite to manage packages, and perform other configuration tasks. It is possible to log in via the serial console without a password but many services such as ssh will require a password set or will not allow root login at all. It is advised to set a root password and create a user account when the unit is first booted.Using a Debian host system will allow for installing a cross compiler to build applications. The advantage of using a Debian host system comes from compiling against libraries. Debian cross platform support allows one to install the necessary development libraries on the host, building the application on the host, and simply installing the runtime libraries on the target device. The library versions will be the same and completely compatible with each other. See the respective Debian cross compiling section for more information.http://www.tis.az/userfiles/caldigit-av-pro-manual.xml

See the Ethernet port section for more information on the switch settings. When the switch is configured for 2 separate networks as it is by default, the eth0 interface should not be directly configured. The switch will provide the eth0.1 and eth0.2 interfaces which can be configured. If the switch is configured to pass through, then the eth0 interface should be used as normal.As an example, to get dhcp from eth0.1This is the server that provides your internet connection. The initrd network configuration does not use this file.If configuring Debian to use DHCP, the file will be automatically overridden by the DHCP client, and no action is necessary.For more information on network configuration in Debian see their documentation here.Before connecting it will show something similar to thisTo connect to the internet or talk to your internal network you will need to configure the interface.The WIFINUSB2 module we provide also supports this mode. Refer to Debians documentation for more details on DHCP configuration.Before packages can be installed, the list of package versions and locations needs to be updated. This assumes the device has a valid network connection to the internet.You can use the aptcache command to search the local cache of Debians packages. You can often find the names of packages from Debians wiki or from just searching on google as well.This assumes you have a network connection to the internet.To regenerate these keysSSH will not allow remote connections without a password or a shared key.This is an example simple startup script that will toggle the red led on during startup, and off during shutdown. In this case Ill name the file customstartup, but you can replace this with your application name as well. However, as long as one of your booting methods still can boot a kernel and the initrd you can rewrite everything by using a usb drive. This is also a good way to blast many stock boards when moving your product into production.

You can find more information about this method with an example script here.Replacing it with an MBR found on a PC would not work as a PC MBR contains an x86 code bootup program.If they are not careful to make sure the OS has not mounted the FS, or existing drivers have ceased any access to the card, they may end up with corruption that is not immediately apparent upon using the card. This may present as sublte corruption, or a card that does not boot at all. We do not encourage use of any other process other than what is described in this section.A USB MicroSD adapter can be used to access the card.Most of the functionality from our software examples can be done from using system calls to run our userspace utilities. Our userspace applications are all designed to go through a TCP interface. By looking at the source for these applications, you can learn our protocol for communicating with the hardware interfaces in any language.Once you get past the initial learning curve it can make you very productive. You can find the vim documentation here.Similar to vim, it is difficult to learn but rewarding in productivity. You can find documentation on emacs here.It doesnt have as many features to assist in code development, but is much simpler to begin using right away. You can find nano documentation here.There are many other commercial compilers which can also be used, but will not be supported by us.The most common way to handle these build systems is using a make file. This lets you define your project sources, libraries, linking, and desired targets. You can read more about makefiles here.You can find an introduction to the autotools here.This is generally simpler than using automake, but is not as mature as the automake tools. You can find a tutorial here.The first of which is gdb part of the gnu compiler collection. This lets you run your code with breakpoints, get backgraces, step forward or backward, and pick apart memory while your application executes.

http://www.drupalitalia.org/node/78137

You can find documentation on gdb here.You can find the manual page here.You can find the manual page here.However, it is also possible to talk to hardware devices from user space. In doing so, one does not have to be aware of the Linux kernel development process. This is the recommended way of accessing hardware on a TSSOCKET system.For testing, this just means the tester needs to be root, which is normal in embedded Linux. For deployment in the field under Debian, this can be an issue because the init process does not have root privileges. To get around this, make sure the binary is owned by root and has the setuid bit set.In the example above, the TS4710 FPGA registers are 16 bits wide, so an unsigned short pointer is used. With very few exceptions, FPGA registers on TSSOCKET macrocontrollers will be 16 bits wide and CPU registers will be 32 bits wide. Unsigned int, unsigned short, and unsigned char pointers should be used for 32, 16, and 8 bit registers, respectively. Otherwise the wrong opcodes may be emitted by the compiler and unexpected behavior will occur. For this board you will want to use this toolchain. To compile your application, you only need to use the version of GCC in the cross toolchain instead of the version supplied with your distribution. The resulting binary will be for ARM.If you want to work with a project, you will typically create a makefile. You can read more about makefiles here. Another common requirement is linking to third party libraries provided by Debian on the board. There is no exact set of steps you can take for every project, but the process will be very much the same. Find the headers, and the libraries. Sometimes you have to also copy over their binaries. In this example, I will link to sqlite from Debian which will also work in the Ubuntu image.You can list the installed files with dpkgThis is not intended to provide any functionality, but just call functions provided by sqlite.

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This will have to be adjusted for your toolchain path.There are many ways to transfer the compiled binaries to the board. Using a network filesystem such as sshfs or NFS will be the simplest to use if you are frequently updating data, but will require more setup. See your linux distributions manual for more details. You can use winscp if from windows, or scp from linux. Make sure you set a password from debian for root or set up a shared key. Otherwise the ssh server will deny connections. From winscp, enter the ip address of the SBC, the root username, and the password you have set or the use of a shared key. This will provide you with an explorer window you can drag files into.Compiling the kernel on the board is not supported or recommended. Before building the kernel you will need to install a few support libraries on your workstationCommonly a reason for recompiling is to add support that was not built into the standard images kernel. You can get a menu to browse available options by runningThis usually takes about 510 minutes.In many cases the OpenJDK JRE is sufficient for an application, but Oracles JRE provides better performance. To install this JRE, first accept the license and download this from Oracle here.The common features will be described in other sections, but for more details see the CPU user guide.The kernel also includes a module that will break this up into partitions. Our default software image contains 2 partitionsThis allows one SD image to be written to two cards allowing redundancy among both SD cards. See our white paper for more information on the concept. Development can take place with a single MicroSD card, but for using DoubleStore 2 MicroSD cards are used.When dual card doublestore is used it stores the same image on both cards and also includes metadata and checksums for the entire image.

http://genesisrealtycorp.com/images/boston-xb4-manual.pdf

The simplest way to get doublestore set up is to first take a backup of your SD image, and then use dblstorctl on a workstation to convert itThis indicates Doublestore has seen the card perform an unexpected behavior that DoubleStore was able to correct.This allows you to receive interrupts from your applications where you would normally have to write a kernel driver. The new irq file allows you to block on a read on the file until an interrupt fires.Currently only three IRQs are used. Offboard IRQs 5, 6, and 7 correspond to FPGA IRQs 0, 1, and 2, respectively. FPGA IRQs 3 to 15 are reserved for future uses. If the DIO pins are not being used as IRQs, they can be masked out by writing 0 to the corresponding bit in the IRQ mask register.It opens the IRQ number specified in the first argument, and prints when it detects an IRQ.This is automatically retrieved on startup, but must be set manually.Its contents will remain with the main power off, so long as the RTC battery is installed and withing a valid voltage range.To set values, the respective environment variable name can be setAt this point, running tshwctl nvram once more will print the updated contents for verification. This can be used for reading a 32bit quantity and updating it with a single command.Both of these can be read using tshwctlThe LEDs have 4 behaviors from default software. The LEDs are also controllable via the Syscon register at offset 0x12.Once it determines this is not a mass storage device the red LED will turn back off.This happens when the system cannot find a valid boot device, or the watchdog is otherwise not being fed. This is normally fed by tshwctl once a valid boot media has started.Typically either the board is not being supplied with enough voltage, or the FPGA has been otherwise damaged. If a stable 5V is being provided and the supply is capable of providing at least 1A to the macrocontroller, an RMA is suggested.

These have various functions depending on the file extensionsThis can be used to have an application automatically run on startup without proceeding with the Linux root filesystems traditionally lengthy startup. This can have an application running within seconds after poweron. As this does not run through the normal startup, any running services or network configuration will need to be started manually.The file will be decompressed and then processed as normal as described in the above table.You will need to have the root.tar downloaded before continuing.Once this is completed, you can reboot to test out the card, or restart the procedure to create another card.This will print out the last 6 of the MAC address which can be used to uniquely identify each board.When in this mode all network traffic should be directed to eth0.1 and eth0.2, but not eth0 which will not be forwarded outside of the switch.In this case the switch is configured to transparently pass through packets rather than configuring the VLANs, so eth0 should be used.This includes the TS8100, TS8390, and TS8900. In this case the Ethernet switch is configured to pass through packets which will only use eth0.In most intended conditions this is OK because the network on either port is never expected to encounter the network on the other. However, there are some very rare network conditions where this situation is possible.See the CPU manual for the complete listing and for information on how to control these DIO.The MFP pins can have multiple functions and not all default to GPIO, so understanding each one you wish to modify is important to your development process. The MFP definition registers are described in the CPU manual starting in Section A1, pages A7 through A12 note these are appendix pages. This wiki will assume the reader already has a thorough understanding of these settings and is comfortable moving forward using them as a GPIO.

NOTE The default TS boot scripts set some MFP pins up with functions other than the default functionality. It is important to set the MFP you wish to use to the function you desire before using it. Do not assume default functionality is present on all MFP pins. The base address for the MFP alternate function block is at 0xD401E000, each MFP pin has its own address as listed in the table starting on page A7. Alternate function definitions start in the table on page 58.Full information on these registers is found in the CPU manual starting at page A832. The GPIO section in the CPU manual contains a typo in the GPIO control base address. The correct base address is 0xD4019000.To use any DIO pin, the direction register must be set 0 for input, 1 for output, then either the input register may be read, or the output register may be written to. These registers are described in the Syscon memory table. Alternatively to read the status of that pin, the Direction Register must be set low, then bit zero of 0x80004020 would reflect the status of that pin.Direction setting 0 is input, 1 is output.This is not required to implement in custom baseboards, but it can be useful to identify the board in software. During startup of the macrocontroller 4 DIO are used to obtain the baseboard model id.Much of the USB OTG framework is described here. You will need to recompile your kernel to include these modules.Because of this the above command needs to be run whenever a USB device is attached to the port in order to tell the OTG driver to enter host mode and communicate with the USB device.Common devices such as keyboards, mice, wifi, and ethernet should mostly work out of the box.This bus also connects to an RTC on the macrocontroller. MFP105 and MFP106 can be used as a second TWI bus directly from the CPU. For more information, see the CPU manual here.

Any external interfaces called for by the TSSOCKET specification that are not provided by the CPU are implemented in the FPGA whenever possible. The FPGA is connected to the CPU by a static memory controller, and as a result the FPGA can provide registers in the CPU memory space.Access to the FPGA is done through either the 8bit or 16bit memory regions. Code should access 16bit or 8bit depending on the access designed for the specific hardware core. For example, the CAN core is 8 bit, the 8 bit MUXBUS space is 8 bit, and some 8 bit cycles are needed for the SPI core if you want to do 8 bit SPI transactions. To access hardware cores in the FPGA, add the offset in the table below to the base address.If we do not have a configuration you need, you can build a new bitstream, or contact us for our engineering services.If interested please contact us.The FPGA bitstream is built using Lattice Diamond which is free and runs under Windows or Linux Redhat. This allows you to modify the verilog and create a jedec file with your custom logic. The jedec is converted to a vme file which is loaded from the SD card and used to reprogram the SRAM of the FPGA on every startup. This requires approximately a second during startup to reprogram, but allows you to recover by removing the bitstream file from the SD card in the case of a faulty bitstream.These sources are supported on the TS4710, TS4712, and TS4720. Custom logic can be built by implementing a wishbone compatible core, or by extending the cores we already have connected. As a simple example these next steps will modify the custom load register located at 0x2a in the syscon.v.On the bottom left there are 3 tabs to control the left panel Files, Process, and Hierarchy. Go to Files, and double click syscon.v. Around line 40 isThe default bitstream will always use 0. This will take approximately 510 minutes. This is used to verify timing of your build.

If timing is not met this will cause seemingly random issues with the bitstream which will usually present first as SD corruption. In order for the board to use this it must be converted to a vme file.The green and red LEDs will shut off during programming, and then turn back on after the bitstream has been reloaded. Commands should not be run during reload since issuing a bus cycle during programming can interfere with timing and cause the reload to fail. Once it has reloaded you can use devmem to verify the register has changedThis register block appears at base address 0x80004000. For example, to identify the modelIf you are using this on your own baseboard this core assumes the standard circuit which allows 2 differential channels and 4 singleended channels.Bits 05 enable channels 16 respectively. The more channels that are enabled, the lower the sampling speed on each channel.This is a pipe that is created in userspace, so for many applications this may provide enough functionality for the watchdog by verifying that userspace is still executing applications. If you would like to have the watchdog functionality more tightly integrated with your application you can specify various feed options.For exampleYou can test Many languages will buffer writes together to make With the TS8100, the CPLD includes all of the DIO and PC104. The MUXBUS timing also influences the communication with PC104 peripherals.For example, to set up a TSSER4 with only jumpers IRQ4, IRQ2, and COM1 setThis can be specified with the iobase argumentThese communicate with the userspace driver xuartctl. Each XUART core in the FPGA can handle up to 8 XUARTs, though the default TS4710 FPGA contains 6. The XUART serial ports have a single shared 4kByte receive FIFO which makes real time interrupt latency response less of a concern and in actual implementation, the serial ports are simply polled at 100Hz and dont even use an IRQ.

An application may simply connect to these ports via localhost or via the network and use the serial ports as if they were network services.For exampleThe mode and baud rate must be set up with xuartctl, and cannot be programatically changed with the standard ioctl.See the xuartctl page for more details on programming with XUARTs. See either of these links for more information on using serial ports in LinuxThis is implemented using SocketCAN.The candump utility can be used to dump all data on the networkThis device will return data from candump withThis shows a simple way you can prove out the communication before moving to another language, but this next example sends the same packet and parses the same response in CYou can find this range at 0x80008000. You must first set the MUXBUS configuration register before accessing this range. For example, to read the board IDMost DIO on this header are rated for 3.3V and are not tolerant of 5V IO. The DIO on this baseboard can be accessed by manipulating the TS8100 Register Map.This example scans the KPAD and prints out the pressed character.These IO are accessed through manipulation of the registers directly.For exampleThe signals for the PC104 are generated by the MAX240 PLD located on the baseboard. It converts the MUXBUS signals from the dual 100pin Macrocontroller interface bus. Pin A1 is nearest to the macrocontroller mounting hole.This can still be set from Debian Used primarily for production. See this file for more information. USB WiFi will not work, and requires a kernel compile and rebuilding the modules as outlined in the Compile the Kernel section. In some cases this could also break the touchscreen loading random data as calibration. This new tshwctl includes locking that will prevent multiple copies from accessing tagmem simultaneously. The 1 CPU USB host still works. You can also contact us for more information.

It has been type tested and found to comply with the limits for a Class A digital device in accordance with the specifications in Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference, in which case the owner will be required to correct the interference at his own expense.Relocate the unit with respect to the receiver. Plug the unit into a different outlet so that the unit and receiver are on different branch circuits. Ensure that mounting screws and connector attachment screws are tightly secured. Ensure that good quality, shielded, and grounded cables are used for all data communications. The following booklets prepared by the Federal Communications Commission FCC may also prove helpfulInterface Handbook Stock No. 0040000045057. These booklets may be purchased from the Superintendent of Documents, U.S. Government Printing Office, Washington, DC 20402.During this warranty period Technologic Systems will repair or replace the defective unit in accordance with the following processThis limited warranty does not cover damages resulting from lightning or other power surges, misuse, abuse, abnormal conditions of operation, or attempts to alter or modify the function of the product.In no event shall Technologic Systems be liable or responsible for any loss or damages, including but not limited to any lost profits, incidental or consequential damages, loss of business, or anticipatory profits arising from the use or inability to use this product.Please, contact Technologic Systems to arrange for any repair service and to obtain repair charge information.Privacy policy About Technologic Systems Manuals Disclaimers. Each channel is configurable for LoZ or HiZ operation, as well as stereo and bridged modes. Advanced Class D technology maximizes efficiency to reduce power consumption and heat dissipation.

An internal universal power supply with power factor correction ensures consistent performance with varying line voltages. Each channel is individually configurable via software for use with “HiZ” distributed speaker systems either 70V or 100V depending on model. Adjacent pairs of channels may be configured for stereo or bridged operation. Stereo mode enables remote control of a stereo pair of speakers using a single set of controls. Bridged mode allows two channels to be combined to provide a single channel delivering 300 watts into 8 ohms. Rear panel input attenuation controls allow for signal level matching. Remote level control and monitoring is enabled using the Crestron Avia Audio Tool software, or using a touch screen control panel or mobile device through integration with a Crestron control system. Integration with a control system also enables centralized monitoring and control of multiple amplifiers throughout a facility as part of a Crestron Fusionmanaged enterprise. Each channel is independently protected, allowing an individual channel to enter protection mode without interrupting the operation of other channels. Protection is automatic, quickly disconnecting the speaker line and shutting down the affected channel, and then restoring normal operation once the fault is resolved. Clear indication of any fault is provided on the front panel, and may also be reported to a control system to provide notification on a touch screen or mobile device, through a text message or email, or at a central help desk using Crestron Fusion. To find a dealer, please contact the Crestron sales representative for your area.Other trademarks, registered trademarks, and trade names may be used in this document to refer to either the entities claiming the marks and names or their products. Crestron disclaims any proprietary interest in the marks and names of others. Crestron is not responsible for errors in typography or photography.

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